Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) A data processing device with an instruction translator comprising:

a processor core; and

a memory interface portion arranged between said processor core and an external memory mapped into a predetermined external memory space,

said memory interface portion including a fetch circuit for receiving an address value for access to said external memory space from said processor core, and fetching information at said address in said external memory, said information being an instruction nonnative to said processor, an instruction native to said processor or data to be processed;

a translator for translating the instruction nonnative to said processor core fetched by said fetch circuit from said external memory into the native instruction; and

a select circuit for selectively applying the information read from said external memory space and the instruction prepared by translating the instruction read from said external memory space by said translator to said processor core depending on whether the address value for the access from said processor core to said external memory space is in a predetermined region or not, wherein

a bus width of an instruction bus in said processor core is different from a bus width of a data bus of said external memory; and

said select circuit includes:

a bus width changing circuit having an input connected to said external memory and an output of the same width as the bus width of the instruction bus of said processor for performing conversion between the bus width of the data bus of said external memory and the bus width of the instruction bus in said processor, and outputting the result, and

a multiplexer having inputs connected to the outputs of said bus width changing circuit and said translator, respectively, and an output connected to said instruction bus of said processor core for selectively applying to said processor core an instruction output from said bus width changing circuit and an instruction output from said translator, depending on whether the address value for the access from said processor core to said external memory space is within a predetermined region or not.

2. (Original) The data processing device with the instruction translator according to claim 1, wherein

said fetch circuit includes:

an address conversion circuit for effecting predetermined conversion on the address for the access from said processor core to said external memory core, and

a circuit for selectively applying the address sent from said processor core and the address output from said address conversion circuit to said external memory depending on whether said address is within said predetermined region or not.

3. (Original) The data processing device with the instruction translator according to claim 2, wherein

said conversion circuit includes a division circuit for dividing the input address value by n-th (n: natural number) power of 2 and outputting the result.

4. (Original) The data processing device with the instruction translator according to claim 3, wherein

said division circuit includes a shifter for shifting rightward the input address value by n bits.

5. (Cancelled)

6. (Currently Amended) The data processing device with the instruction translator according to claim 1, wherein

said processor core has an instruction bus, an instruction address bus, a data bus and a data address bus, and

said data processing device further includes:

a second multiplexer having inputs connected to said instruction address bus and said data address bus, respectively, for selecting said instruction address bus or said data address bus for application to said fetch circuit in response to the control signal applied from said processor core, and

a ~~second~~ third multiplexer for electrically coupling said memory bus to said instruction bus or said data bus, in response to said control signal applied from said processor core.

7. (Currently Amended) A memory interface device with instruction translator to be arranged between a processor core and an external memory mapped into a predetermined external memory space, comprising:

a fetch circuit for receiving an address value for access to said external memory space from said processor core, and fetching information at said address in said external memory, said information being an instruction nonnative to said processor, an instruction native to said processor, or data to be processed;

a translator for translating the instruction nonnative to said processor core fetched by said fetch circuit from said external memory into the instruction native to said processor; and

a select circuit for selectively applying the information read from said external memory space and the instruction prepared by translating the instruction read from said external memory space by said translator to said processor core depending on whether the address value for the access from said processor core to said external memory space is in a predetermined region or not, wherein

a bus width of an instruction bus in said processor core is different from a bus width of a data bus of said external memory; and

said select circuit includes:

a bus width changing circuit having an input connected to said external memory and an output of the same width as the bus width of the instruction bus of said processor, for performing conversion between the bus width of the data bus of said external memory and the bus width of the instruction bus in said processor, and outputting the result, and

a multiplexer having inputs connected to the outputs of said bus width changing circuit and said translator, respectively, and an output connected to said instruction bus of said processor

core for selectively applying to said processor core an instruction output from said bus width changing circuit and an instruction output from said translator depending on whether the address value for the access from said processor core to said external memory space is within a predetermined region or not.

8. (Original) The memory interface device with the instruction translator according to claim 7, wherein

said fetch circuit includes:

an address conversion circuit for effecting predetermined conversion on the address for the access from said processor core to said external memory core, and

a circuit for selectively applying the address sent from said processor core and the address output from said address conversion circuit to said external memory depending on whether said address is within said predetermined region or not.

9. (Original) The memory interface device with the instruction translator according to claim 8, wherein

said conversion circuit includes a division circuit for dividing the input address value by n-th (n: natural number) power of 2 and outputting the result.

10. (Original) The memory interface device with the instruction translator according to claim 9, wherein

said division circuit includes a shifter for shifting rightward the input address value by n bits.

11. (Cancelled)

12. (Currently Amended) The memory interface device with the instruction translator according to claim 7, wherein

said processor core has an instruction bus, an instruction address bus, a data bus and a data address bus, and

said data processing device further includes:

a second multiplexer having inputs connected to said instruction address bus and said data address bus, respectively, for selecting said instruction address bus or said data address bus for application to said fetch circuit in response to the control signal applied from said processor core, and

a ~~second~~ third multiplexer for electrically coupling said memory bus to said instruction bus or said data bus in response to said control signal applied from said processor core.

13. (Currently Amended) A data reading method for reading information from an external memory mapped into a predetermined external memory space to a processor core, comprising the steps of:

receiving an address value for access from said processor core to said external memory space, and fetching the information at said address in said external memory, said data being an instruction nonnative to said processor, an instruction native to said processor, or data to be processed;

translating the instruction nonnative to said processor core fetched from said external memory into the instruction native to the processor; and

selectively applying the information read from said external memory space and the instruction prepared by the translation of the instruction read from said external memory space to said processor core depending on whether the address value for the access from said processor core to said external memory space is in a predetermined region or not, wherein

a bus width of an instruction bus in said processor core is different from a bus width of a data bus of said external memory; and

said selectively applying step includes the steps of:

changing the data width of the fetched information by said external memory to the bus width of the instruction bus within said processor core, and

selectively applying to said processor core the information having the changed bus width and the translated native instruction depending on whether the address value for the access from said processor core to said external memory space is within a predetermined region or not.

14. (Original) The data reading method according to claim 13, wherein

said fetching step includes the steps of:

effecting predetermined conversion on the address for the access from said processor core to said external memory core, and

selectively applying the address sent from said processor core and the address subjected to said predetermined conversion to said external memory depending on whether said address is within said predetermined region or not.

15. (Original) The data reading method according to claim 14, wherein

said converting step includes a step of dividing the input address value by n-th (n: natural number) power of 2 and outputting the result.

16. (Original) The data reading method according to claim 15, wherein

said dividing and outputting step includes a step of shifting rightward the input address value by n bits.

17. (Cancelled)

18. (Original) The data reading method according to claim 13, wherein

said processor core has an instruction bus, an instruction address bus, a data bus and a data address bus, and

said data reading method further includes the steps of:

selecting the address on said instruction address bus or the address on said data address bus for inputting the selected address to said fetching step in response to the control signal applied from said processor core, and

electrically coupling said memory bus to said instruction bus or said data bus in response to said control signal applied from said processor core.